Miniature, 1-W, 1500-Vrms Isolated Unregulated DC-DC Converters

FEATURES

- **Up To 85% Efficiency**
- **Thermal Protection**
- **Device-to-Device Synchronization**
- **Short-Circuit Protection**
- **EN55022 Class B EMC Performance**
- **UL1950 Recognized Component**
- **JEDEC PDIP-14 and Gull-Wing Packages**

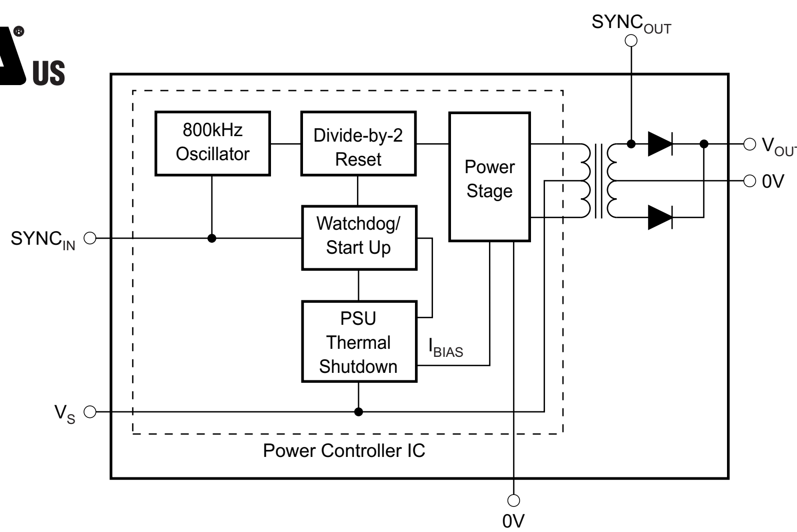
APPLICATIONS

- **Industrial Control and Instrumentation**
- **Point-of-Use Power Conversion**
- **Ground Loop Elimination**
- **Data Acquisition**
- **Test Equipment**
- **Secondary Isolation Circuits**

DESCRIPTION

The DCV01 series is a family of 1-W, 1500-Vrms isolated, unregulated dc-dc converters. Requiring a minimum of external components and including on-chip device protection, the DCV01 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with a power density of 40 W/in^3 (2.4 W/cm^3). This combination of features, high isolation, and small size makes the DCV01 suitable for a wide range of applications.



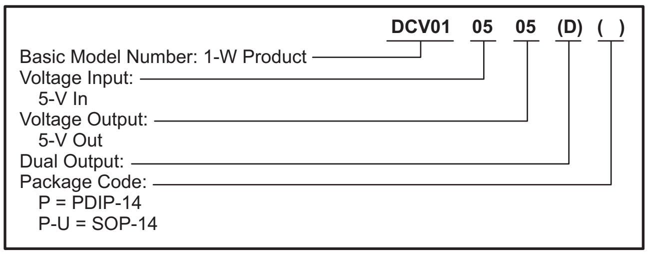
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or visit the device product folder at www.ti.com.

SUPPLEMENTAL ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage	5-V input models	7	V
	15-V input models	18	V
	24-V input models	29	V
Storage temperature range		–60 to +125	°C
Lead temperature (soldering, 10 s)		+270	°C

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT					
Power	100% full load		0.97		W
Ripple	O/P capacitor = 1-μF, 50% load		20		mV_{PP}
Voltage vs temperature	Room to cold		0.046		%/°C
	Room to hot		0.016		%/°C
INPUT					
Voltage range on V_S		–10%		10%	
ISOLATION					
Voltage	1-s flash test	1.5			kVrms
	UL1950[(1)]	1.5			kVrms
LINE					
Regulation			1		%/1% of V_S
SWITCHING/SYNCHRONIZATION					
Oscillator frequency (f_{OSC})	Switching frequency = f_{OSC} / 2		800		kHz
Sync input low [(2)]		0		0.4	V
Sync input current [(2)]	V_{SYNC} = +2 V		75		μA
Disable time			2		μs
Capacitance loading on $SYNC_{IN}$ pin	External			3	pF
RELIABILITY					
Demonstrated	T_A = +55°C			75	FITS
THERMAL SHUTDOWN					
IC temperature at shutdown			+150		°C
Shutdown current			3		mA
TEMPERATURE					
Operating range		–40		+85	°C

(1) During UL1950 recognition test only. UL file # E199929.
(2) For more information on synchronization, refer to Application Report SBAA035., *External Synchronization of the DCP01/02, DCR01/02, and DCV01 Series of DC/DC Converters*.

ELECTRICAL CHARACTERISTICS PER DEVICE

At T_A = +25°C, unless otherwise noted.

	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			LOAD REGULATION (%)		NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)	LEAKAGE CURRENT (μA)
	V_S			V_{NOM}					I_Q		C_{ISO}	
				75% LOAD[(1)]			10% TO 100% LOAD[(2)]		0% LOAD	100% LOAD	V_{ISO} = 750 Vrms	V_{ISO} = 750 Vrms
PRODUCT	MIN	TYP	MAX	MIN	TYP	MAX	TYP	MAX	TYP	TYP	TYP	TYP
DCV010505	4.5	5	5.5	4.75	5	5.25	23	31	20	78	3.6	0.9
DCV010505D	4.5	5	5.5	±4.25	±5	±5.75	19	32	23	80	3.8	0.9
DCV010512	4.5	5	5.5	11.4	12	12.6	23	38	30	85	5.1	1.2
DCV010512D	4.5	5	5.5	±11.4	±12	±12.6	19	37	40	82	4.0	1.0
DCV010515	4.5	5	5.5	14.25	15	15.75	30	42	34	84	3.8	0.9
DCV010515D	4.5	5	5.5	±14.25	±15	±15.75	27	41	42	85	4.7	1.1
DCV011512D	13.5	15	16.5	±11.4	±12	±12.6	11	39	19	78	4.2	1.0
DCV011515D	13.5	15	16.5	±14.25	±15	±15.75	12	39	20	79	4.2	1.0
DCV012405	21.6	24	26.4	4.75	5	5.25	13	23	14	77	3.8	0.9
DCV012415D	21.6	24	26.4	±14.25	±15	±15.75	12	35	17	76	5.3	1.3

(1) 100% load current = 1 W/V_{NOM} typical.
(2) Load regulation = (V_{OUT} at 10% – V_{OUT} at 100%)/V_{OUT} at 75%.

PIN CONFIGURATION: SINGLE OUTPUT

NVA AND DUA PACKAGES
PDIP-14 AND SOP-14
(TOP VIEW)

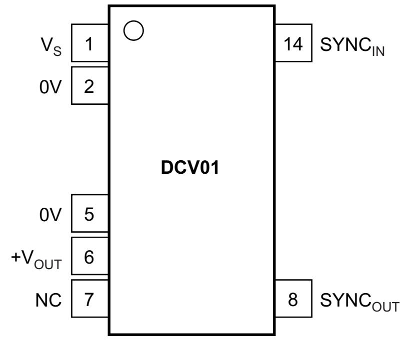


Table 1. Pin Descriptions (Single Output)

PIN NAME	PIN NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
NC	7	Not connected
$SYNC_{OUT}$	8	Unrectified transformer output
$SYNC_{IN}$	14	Synchronization pin

PIN CONFIGURATION: DUAL OUTPUT

NVA AND DUA PACKAGES
PDIP-14 AND SOP-14
(TOP VIEW)

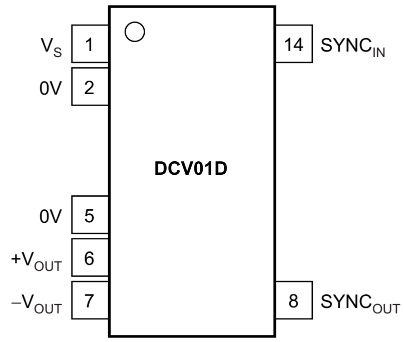


Table 2. Pin Descriptions (Dual Output)

PIN NAME	PIN NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
$–V_{OUT}$	7	–Voltage out
$SYNC_{OUT}$	8	Unrectified transformer output
$SYNC_{IN}$	14	Synchronization pin

TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

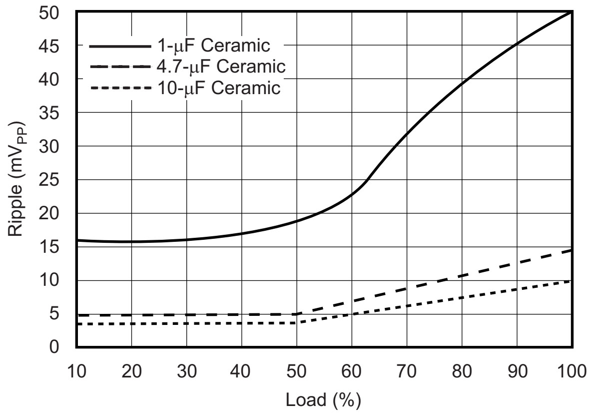


Figure 1. DCV010505 OUTPUT RIPPLE vs LOAD (20-MHz BW)

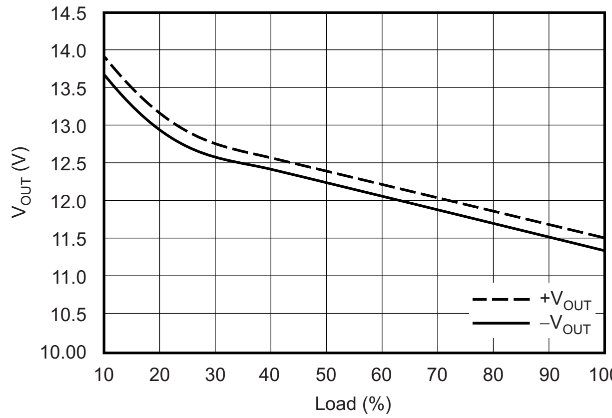


Figure 2. DCV010512D V_{OUT} vs LOAD

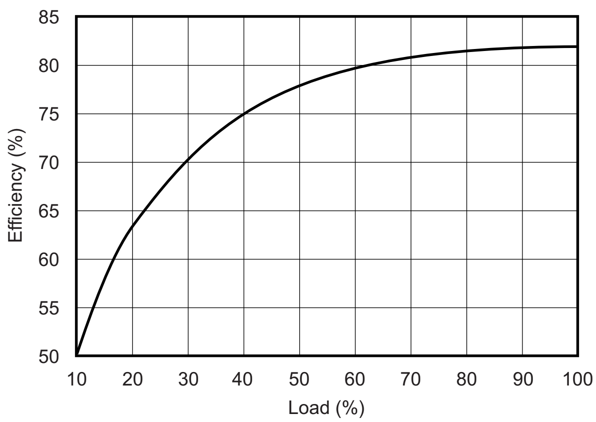


Figure 3. DCV010512D EFFICIENCY vs LOAD

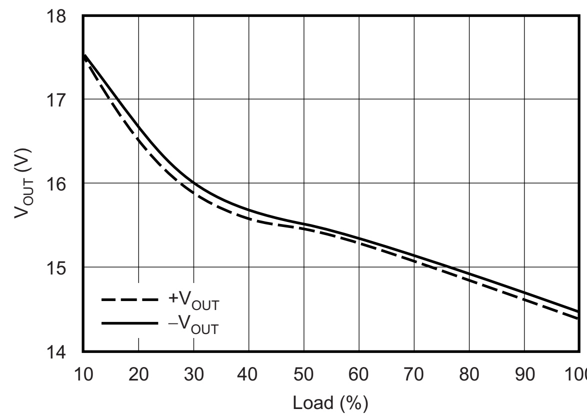


Figure 4. DCV010515D V_{OUT} vs LOAD

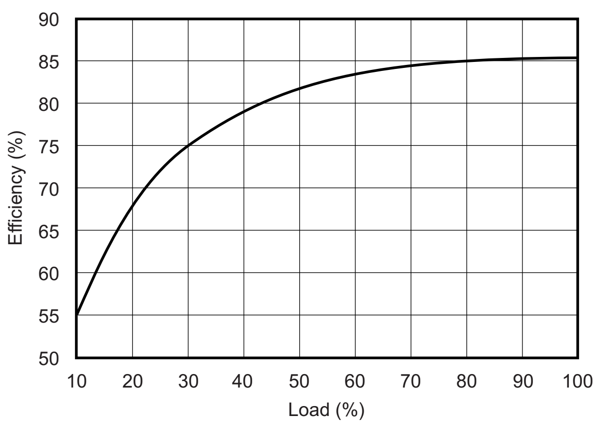


Figure 5. DCV010515D EFFICIENCY vs LOAD

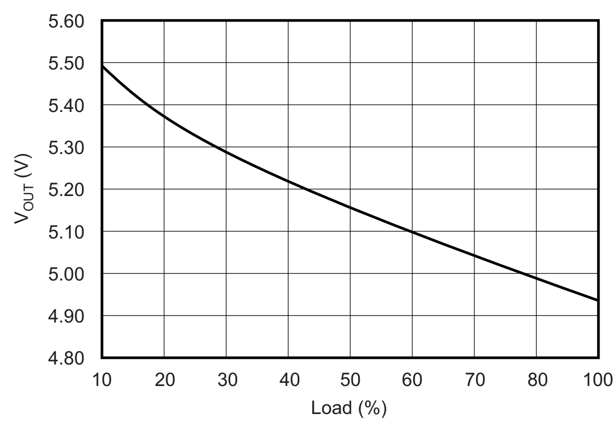


Figure 6. DCV012405 V_{OUT} vs LOAD

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

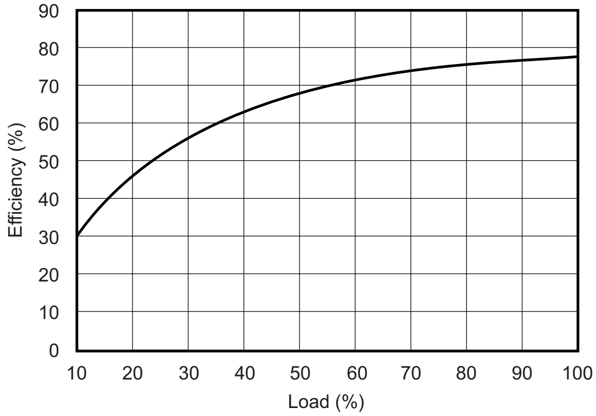


Figure 7. DCV012405 EFFICIENCY vs LOAD

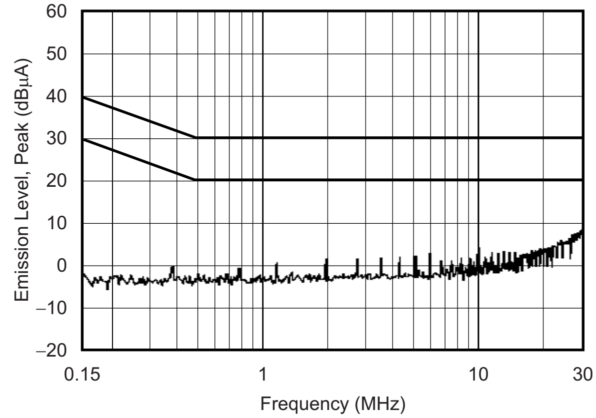


Figure 8. DCV010505 CONDUCTED EMISSIONS (125% Load)

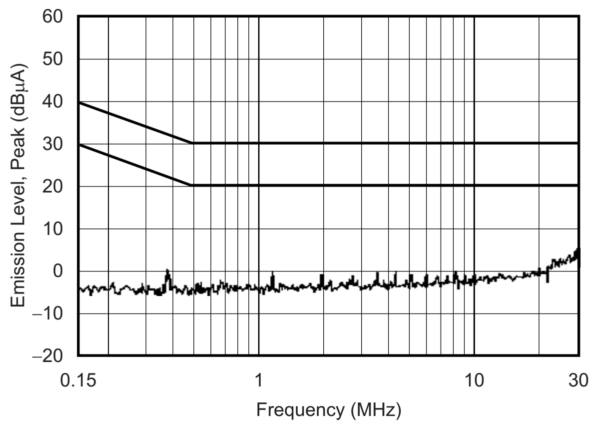


Figure 9. DCV010505 CONDUCTED EMISSIONS (8% Load)

FUNCTIONAL DESCRIPTION

OVERVIEW

The DCV01 offers up to 1 W of unregulated output power with a typical efficiency of up to 85%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process. Separate primary and secondary transformer windings give good isolation and low barrier capacitance.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400 kHz (divide-by-2 from 800-kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCV01 circuits or an external source, and is used to minimize system noise. A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the $SYNC_{IN}$ pin low. The output pins will be tri-stated. This will occur in 2 µs.

THERMAL SHUTDOWN

The DCV01 is protected by a thermal-shutdown circuit. If the on-chip temperature exceeds 150°C, the device will shut down. Once the temperature falls below 150°C, normal operation will resume.

SYNCHRONIZATION

In the event that more than one dc-dc converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the dc-dc converters.

The DCV01 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the $SYNC_{IN}$ pins together, taking care to minimize the capacitance of tracking. Stray capacitance (> 3 pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit.

It should be noted that if synchronized devices are used at start up, all devices will draw maximum current simultaneously. This can cause the input voltage to dip, and if it dips below the minimum input voltage (4.5 V), the devices may not start up. A 2.2-µF capacitor should be connected close to the input pins. If more than eight devices are to be synchronized, it is recommended that the $SYNC_{IN}$ pins are driven by an external device. Details are contained in Application Report SBAA035, *External Synchronization of the DCP01/02 Series of DC/DC Converters*, available for download from www.ti.com.

CONSTRUCTION

The basic construction of the DCV01 is the same as standard ICs. There is no substrate within the molded package. The DCV01 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCV01 does not require any special printed circuit board (PCB) assembly processing. This results in an isolated dc-dc converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCV01 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCV01 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2 μs. Removal of the pull down will cause the DCV01 to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400 kHz allows simple filtering. To reduce ripple, it is recommended that at least a 1-μF ceramic capacitor is used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2-μF low-ESR ceramic capacitor on the input of the 5-V input versions, and a 0.47-μF low ESR cap on the 24-V input versions is recommended.

Connecting the DCV01 in Series

Multiple DCV01 isolated 1W dc-dc converters can be connected in series to provide nonstandard voltage rails. This is possible by using the floating outputs provided by the galvanic isolation of the DCV01.

Connect the positive V_{OUT} from one DCV01 to the negative V_{OUT} (0 V) of another, as shown in Figure 10. If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCV01 will prevent beat frequencies on the voltage rails. The $SYNC_{IN}$ feature of the DCV01 allows easy series connection without external filtering, thus minimizing cost. The outputs on the dual-output DCV01 versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 11. For example, a dual 15-V DCV01 could be connected to provide a 30-V rail.

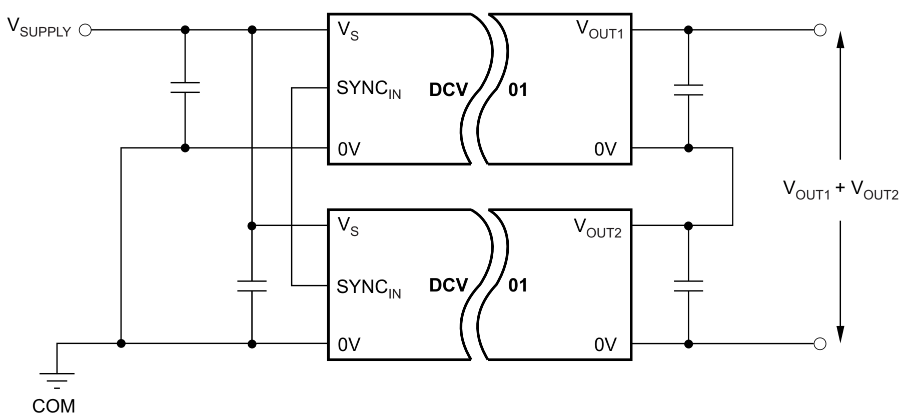


Figure 10. Connecting the DCV01 in Series

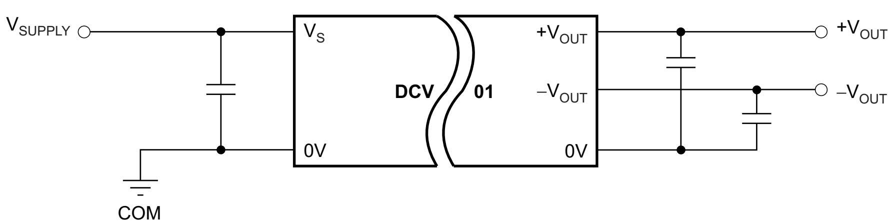


Figure 11. Connecting Dual Outputs in Series

Connecting the DCV01 in Parallel

If the output power from one DCV01 is not sufficient, it is possible to parallel the outputs of multiple DCV01s, as shown in Figure 12. Again, the $SYNC_{IN}$ feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

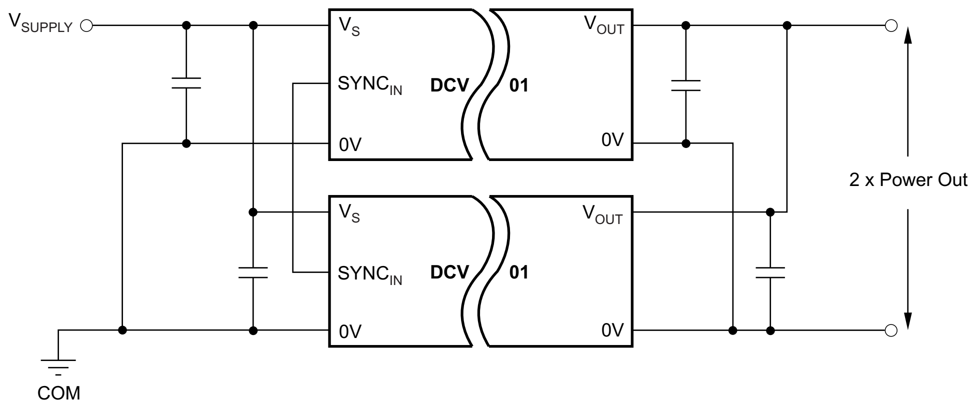


Figure 12. Connecting Multiple DCV01s in Parallel

PCB LAYOUT

RIPPLE AND NOISE

Careful consideration should be given to the layout of the PCB in order that the best results can be obtained.

The DCV01 is a switching power supply, and as such, can place high peak-current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to track the power to the input of the DCV01. If this is not possible, then the supplies must be connected in a star formation with the tracks made as wide as possible.

If the $SYNC_{IN}$ pin is being used, then the tracking between device $SYNC_{IN}$ pins should be short, in order to avoid stray capacitance. If the $SYNC_{IN}$ pin is not being used, it is advisable to place a guard ring, (connected to input ground) around this pin to avoid any noise pick up.

The output should be taken from the device using ground and power planes; this will ensure minimum losses.

A good quality low-ESR capacitor placed as close as practicable across the input will reduce reflected ripple and ensure a smooth start up.

A good quality low-ESR capacitor placed as close as practicable across the rectifier output terminal and output ground will give the best ripple and noise performance.

THERMAL MANAGEMENT

Due to the high power density of this device, it is advisable to provide ground planes on the input and output.

ISOLATION

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety Extra Low Voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42V peak or 60VDC for more than 1 second.

DCH, DCP, DCR, and DCV Series DC-DC Converters

TI’s DCH, DCP, DCR, and DCV (DCx) series dc-dc converters are specified for operational isolation only.

Operation or Functional Isolation

Operational or functional isolation is defined by the use of a hipot test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation should never be used as an element in a safety-isolation system.

Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.4 V peak, or 60 VDC; that is, both input and output should normally be maintained within SELV limits. The isolation test voltage represents a measure of immunity to transient voltages; do not use the device as an element of a safety isolation system when SELV is exceeded. If the device is expected to function correctly with more than 42.4 V peak or 60 VDC applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

Isolation Voltage

Hipot test, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation.

TI’s DCx series of dc-dc converters are all 100% production tested at their stated isolation voltage.

For the DCP and DCR series, this voltage is 1.0 kVDC for one second.

For the DCV series, this voltage is 1.5 kVDC for one second.

For the DCH series, this voltage is 3.5 kVDC for one second.

Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCx series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2000) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCV010505DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010505DP	Samples
DCV010505DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010505DP-U	Samples
DCV010505P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010505P	Samples
DCV010505P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010505P-U	Samples
DCV010505P-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010505P-U	Samples
DCV010512DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010512DP	Samples
DCV010512DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV10512DPU	Samples
DCV010512P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010512P	Samples
DCV010512P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010512P-U	Samples
DCV010515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010515DP	Samples
DCV010515DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010515DP-U	Samples
DCV010515P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV010515P	Samples
DCV010515P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV010515P-U	Samples
DCV011512DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV011512DP	Samples
DCV011512DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV011512DP-U	Samples
DCV011515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV011515DP	Samples
DCV011515DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV011515DP-U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCV011515DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV011515DP-U	Samples
DCV012405P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV012405P	Samples
DCV012405P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV012405P-U	Samples
DCV012405P-U/700	OBSOLETE	SOP	DUA	7		TBD	Call TI	Call TI		DCV012405P-U	
DCV012415DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCV012415DP	Samples
DCV012415DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV012415DP-U	Samples
DCV012415DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCV012415DP-U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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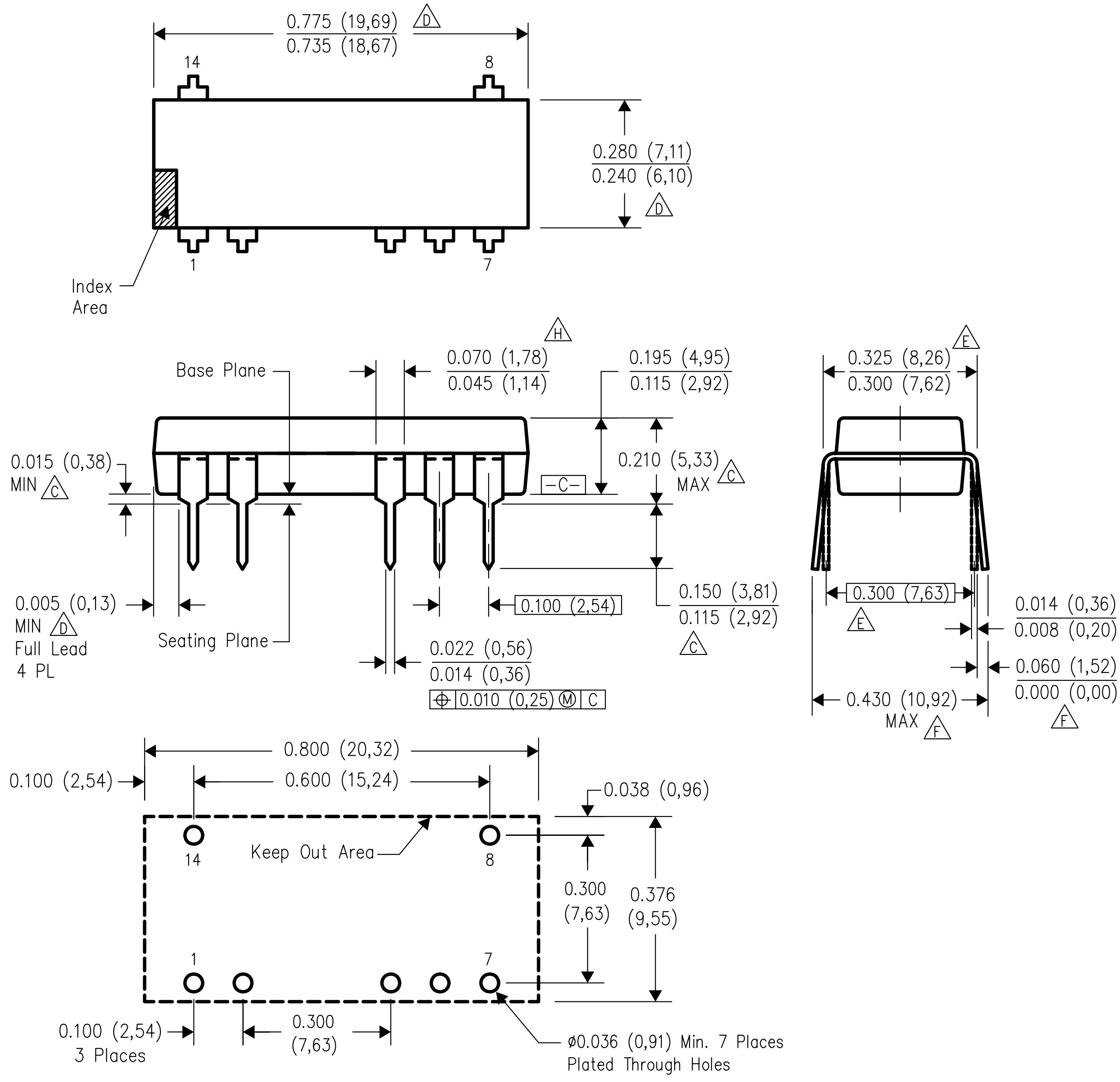
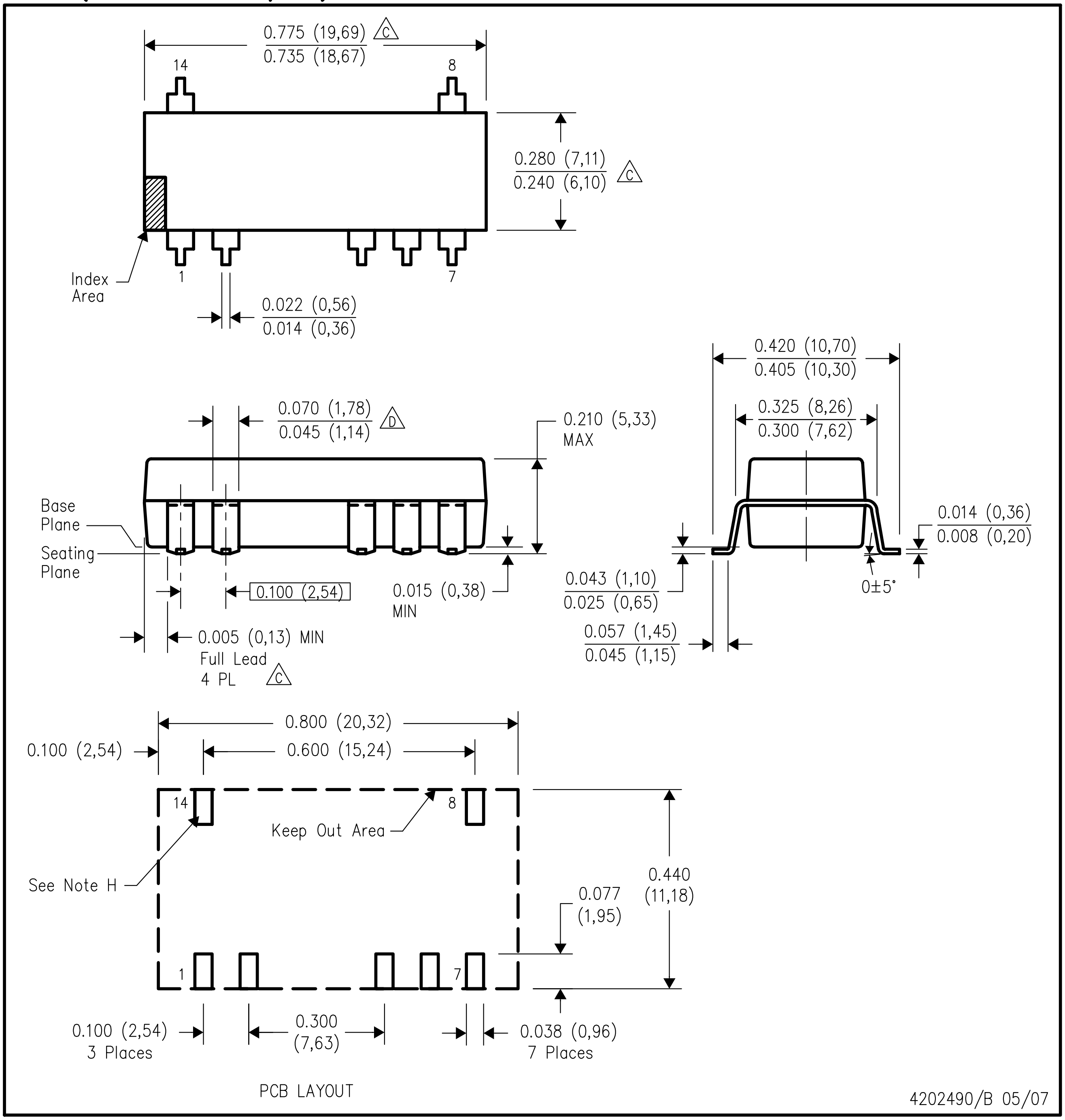
NVA (R-PDIP-T7/14) PLASTIC DUAL-IN-LINE



4202489/B 05/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross-hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS-001-AA.

DUA (R–PDSO–G7/14) PLASTIC SMALL–OUTLINE



NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).

D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed exceed 0.010 (0,25).

E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.

F. A visual index feature must be located within the cross–hatched area.

G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

H. Power pin connections should be two or more vias per input, ground and output pin.

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